REMARKS

This is a full and timely response to the Office Action dated February 8, 2006. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this Response, claims 1-2, 4-8, 10-16, 18-27, 31, and 32 are pending in this application. Claims 7, 11, 16, and 19 have been directly amended via amendments set forth herein, and claim 30 has been cancelled. Further, claims 31 and 32 are newly added. It is believed that the foregoing amendments add no new matter to the present application.

Claim Objections

Claims 7, 11, 19 are objected to due to alleged informalities. Applicant asserts that claims 7, 11, and 19 are directly amended herein thereby making the objection to this claim moot. Accordingly, Applicant respectfully requests that the objections to claims 7, 11, and 19 be withdrawn.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981). In addition, "(t)he PTO has the burden under section 103 to establish a *prima facie* case of obviousness.

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 1 reads as follows:

> 1. A computer system for efficiently executing instructions of computer programs, comprising:
>
> processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;
>
> cache memory;
>
> computer memory having a plurality of addresses; and
>
> memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to store, in response to said first context switch command, in computer memory, data written by said pipeline during execution of said one program and to store an indicator indicative of whether said data was accessed by the processing circuitry during a particular time period prior to said first context switch in executing said instructions from said one program, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing said indicator corresponding to said data previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, said ***memory control circuitry further configured to make a determination, based on said indicator, whether said data was accessed by the processing circuitry in the particular time period prior to the first context switch for determining whether to preload said data into said cache memory in response to said second context switch, to retrieve said data, based upon said determination, from said computer memory in response to said second context switch command, and to store said retrieved data in said cache memory based upon said indicator.*** (Emphasis added).

Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* fails to teach or suggest at least the features of claim 1 highlighted hereinabove.

In particular, the Office Action states *Lass* does not teach but that *Tremblay*

> "teaches the details to partially saving and restoring data with memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to store, in response to said first context switch command, in computer memory, data written by said pipeline during execution of said one program and to store an indicator indicative of whether said data was accessed by the processing circuitry

during a particular time period prior to said first context switch in executing said instructions from said one program, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing said indicator corresponding to said data previously written by said pipeline during execution of an instruction of said one computer program prior to said first context switch, said memory control circuitry further configured to make a determination, based on said indicator, whether said data was accessed by the processing circuitry in the particular time period prior to the first context switch for determining whether to preload said data into said cache memory in response to said second context switch, to retrieve said data, based upon said determination, from said computer memory in response to said second context switch command, and to store said retrieved data in said cache memory based upon said indicator."

Applicant respectfully traverses such assertion.

In this regard, *Tremblay* appears to teach a system that comprises a set of bits identified as "dirty bit storage...that holds an access history of registers in the register file." See column 10, lines 45-48. "If the register or register group [associated with one of the bits in the dirty bit storage] has been written...a value in the dirty bit storage...designates the written condition of the register or group of registers." See columns 10, lines 52-60. *Tremblay* appears to teach that the "dirty bit enable storage...bit values...disable or enable access to the register or group of registers that correspond to each [dirty] bit." See column 11, lines 49-52.

Thus, **access** to the registers is controlled based on the written condition designated by the dirty bit storage. However, *Tremblay* fails to suggest that the data in the registers is preloaded to the registers "in response to a context switch command." Accordingly, the Office Action fails to establish that the cited art suggests at least "memory control circuitry further configured to preload said data into said cache memory ***in response to said second context switch***" as described by claim 1. (Emphasis added).

In addition, there is nothing in Tremblay to suggest that data is "preloaded" to the registers. In this regard, it appears that data is stored to the registers when the program being executed writes the data to the registers. Such writing of data by the

program being executed does not constitute "preloading" of the registers. Thus the cited art fails to support "determining whatever to preload such data into said cache memory," as described by claim 1.

For at least the reasons set forth above, Applicant respectfully submits that the combination of *Lass* and *Tremblay* does not teach or suggest at least those limitations highlighted in amended claim 1. Therefore, Applicant respectfully submits that the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

Claims 2, 4-6, 31 and 32

Claims 2 and 4-6 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay,* and claims 31 and 32 are newly added. Applicant submits that the pending dependent claims 2, 4-6, 31 and 32 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2, 4-6, 31 and 32 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 7 reads as follows:

> 7. A computer system for efficiently executing instructions of computer programs, comprising:
> processing circuitry having a pipeline, said pipeline configured to execute instructions from one of a plurality of programs, said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command;
> cache memory;
> computer memory having a plurality of addresses; and

memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to maintain a plurality of mappings, said mappings respectively correlating at least one data value previously written by said pipeline during execution of an instruction and stored in said cache memory with said memory addresses of said computer memory, ***said memory control circuitry configured to store in said computer memory said mappings and information indicating whether said at least one data value was recently accessed and to make a determination, based on said information, whether said information indicates that said at least one data value was recently accessed prior to the first context switch, said memory control circuitry further configured to preload, into said cache memory, said at least one data value based on said determination if said information indicates that said at least one data value was recently accessed prior to said first context switch.*** (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* does not teach or suggest the highlighted features of claim 7 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 7 be withdrawn.

Claims 8 and 10-11

Claims 8 and 10-11 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Applicant submits that the pending dependent claims 8 and 10-11 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8 and 10-11 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 7.

Claim 12

Claim 12 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 12 reads as follows:

12. A method for efficiently executing instructions of computer programs, comprising the steps of:

executing a plurality of computer programs in an interleaved fashion;

switching which of said computer programs is being executed in said executing step;

storing, prior to said switching step, at an address in computer memory a data value previously written by a pipeline to a cache line in execution of an instruction corresponding to one of said computer programs in said executing step and an indicator indicating if the cache line was recently accessed ;

identifying said address in response to said switching step;

determining, based on said indicator, whether the data value was recently accessed prior to said switching step;

retrieving, based on said determining step, said data value from said address based on said identifying step and in response to said switching step if said indicator indicates that the data was recently accessed; and

storing said retrieved data value in cache memory. (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* does not teach or suggest the highlighted features of claim 12 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 12 be withdrawn.

Claims 13-15

Claims 13-15 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay.* Applicant submits that the pending dependent claims 13-15 contain all features of their respective independent claim 12. Since claim 12 should be allowed, as argued hereinabove, pending dependent claims 13-15 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 12.

Claim 16

Claim 16 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 16 reads as follows:

> 16. A method for efficiently executing instructions of computer programs, comprising the steps of:
> executing instructions from a computer program;
> halting said executing step during a first context switch in response to a first context switch command;
> resuming said executing step during a second context switch in response to a second context switch command;
> maintaining a plurality of mappings;
> correlating, via said mappings, data values previously written by a pipeline during the executing step and stored in a cache memory with memory addresses of computer memory outside of said cache memory;
> storing said mappings in said computer memory in response to said first context switch command and information indicative of whether said data values were accessed during a particular time period prior to said first context switch;
> ***selecting, based on said information and for preloading into the cache memory in response to the second context switch command, at least one data value from at least one of said addresses identified by said mappings; and***
> ***retrieving, based on said mappings and said selecting step, said at least one data value in response to said second context switch command if said information indicates that said at least one data value was accessed during said particular time period; and***
> ***storing said at least one retrieved data value in said cache memory.*** (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* does not teach or suggest the highlighted features of claim 16 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 16 be withdrawn.

Claims 18 and 19

Claims 18 and 19 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Applicant submits that the pending dependent claims 18 and 19 contain all features of their respective independent claim 16. Since claim 16 should be allowed, as argued hereinabove, pending dependent claims 18 and 19 should be allowed as a

matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 16.

Claim 20

Claim 20 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 20 reads as follows:

> 20. A computer system for efficiently executing instructions of computer programs, comprising:
> computer memory; and
> a processing unit comprising cache memory and logic configured to store in said computer memory a value indicative of whether a portion of said cache memory was recently accessed by said processor and a mapping associated with said value, ***said mapping indicative of a location in said computer memory storing data previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process, the logic further configured to select said data for preloading in said cache memory after said second context switch if said value indicates that the data was recently accessed, retrieve said data based on said value and store said data in said cache if said value indicates that the data was recently accessed, said processing unit continuing execution of said first process with the retrieved data when the processing unit context switches out the second process and context switches in the first process.*** (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 1, Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* does not teach or suggest the highlighted features of claim 20 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 20 be withdrawn.

Claim 20

Claim 20 presently stands rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Claim 20 reads as follows:

> 21. A method for efficiently executing instructions of computer programs, comprising the steps of:
> storing a value indicative of whether data in cache memory was recently accessed by a processing unit;
> storing in said memory a mapping corresponding to said value, said mapping indicative of a location in computer memory storing said data when the processing unit context switches out the first process for processing of a second process;
> determining whether said data was recently accessed prior to said processing unit switching out the first process;
> ***preloading, based on said determining step, said data in said cache for execution of said first process by said processing unit if said value indicates that the data was recently accessed in said determining step.*** (Emphasis added).

For at least the reason set forth hereinabove with reference to claim 12, Applicant respectfully asserts that the alleged combination of *Lass* and *Tremblay* does not teach or suggest the highlighted features of claim 21 hereinabove. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103 rejection of claim 21 be withdrawn.

Claims 22-27

Claims 22-27 presently stand rejected under 35 U.S.C. §103 as unpatentable over *Lass* in view of *Tremblay*. Applicant submits that the pending dependent claims 22-27 contain all features of their respective independent claim 21. Since claim 21 should be allowed, as argued hereinabove, pending dependent claims 22-27 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 21.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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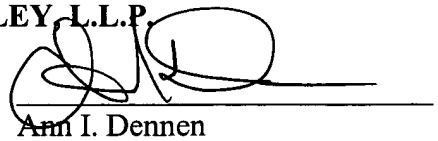
By: 

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